論 文 の 要 約

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Among the many potential hardware platforms, superconducting quantum circuits have become the leading contender for constructing a scalable quantum computing system.　Not only have we seen significant advances in recent years in reliable fabrication and control technology, but the quality of the qubits themselves have increased by many orders of magnitude. Almost all current architecture designs necessitate a two-dimensional arrangement of superconducting qubits with nearest-neighbor interactions, that is compatible with powerful quantum error-correction using the surface code. A major hurdle for scalability in superconducting systems is the so-called wiring problem, where internal qubits of a chipset become inaccessible for external control/readout lines.

The current consensus within the superconducting quantum circuit field is that the control wiring for such chips should be fabricated in the third dimension, utilizing several techniques to place bias, readout and control wires orthogonal to the plane of the chip itself.　This technique has shown much promises, but it is also very unclear and still a significant engineering challenge if these intricate, three-dimensional wiring and packaging technology control fabrication techniques are compatible with maintaining high fidelity operations and increasing chip size. The largest concern is the ability to reduce cross-talk and control line contamination of neighbouring qubits to the degree necessary to achieve fidelities of 99% or higher across the chip. In other words, these approaches resort to intricate, three-dimensional wiring and packaging technology, which is a significant engineering challenge to realize while maintaining qubit fidelity.

In this thesis, we present a revolutionary new large-scale micro-architecture design that completely side-steps this issue. We propose a pseudo-2D arrangement architecture of superconducting qubits. This bi-linear array allows each physical qubit to be biased, measured and controlled using wiring that remains in-plane with the chip (eliminating completely the need for 3D control line fabrication and packaging).

Utilizing the micro-architecture bi-linear arrangement of superconducting qubits, we also show how a large Raussendorf cluster can be produced, which realizes the cluster state model of surface code quantum error correction while maintaining planar access of control lines to each individual qubit.　This architecture realizes the cluster state model of surface code quantum error correction, without the need for 3-dimensional control wiring. Moreover, we propose that

bi-linear transformed arrangement with additional qubits can be generate a 3D-cluster-state on completely planer circuit with some overhead.

A novel architecture for superconducting circuits is also proposed to improve the efficiency of a quantum annealing system. To increase the capability of a circuit, it is desirable for a qubit to be coupled not only with adjacent qubits but also with other qubits located far away. We introduce a circuit that uses a lumped element resonator coupled each with one qubit. The resonator-qubit pairs are coupled by rf-superconducting quantum interference device (SQUID) based couplers. These pairs make a large quantum system for quantum annealer. This system could prepare the problem Hamiltonian and tune the parameters for quantum annealing procedure.